UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,787	07/19/2000	MAKOTO TODA	NIT-195	4755

24956	7590	03/30/2004

MATTINGLY, STANGER & MALUR, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER
MCLEAN MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	16

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/530,787	TODA ET AL.
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2003*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-35 and 37-39* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-21* is/are allowed.

6)☒ Claim(s) *1-8,10-17,22-35 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
   application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

1.   The enclosed detailed action is in response to the Amendment submitted on October 10,

2003 and Applicant's request for a new office action and reset of statutory due date.

In response to Applicant's request for a new office and to reset the statutory due date, the

enclosed office action is in response to the Amendment submitted on October 10, 2003. The

Examiner did not find a Supplemental Amendment submitted on October 30, 2003 in the file.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claim 1, 5-6, 26 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Sharma et al. (USPN: 5,960,463) in view of Takagi (USPN: 5,440,708).

Regarding claims 1, 6, 26 and 31, Sharma discloses a data processor comprising a CPU for

outputting a first address (Figure 2A- logic within Reference 120 which provides an address to

Reference 210); address translations means for inputting the first address, translating the first

address to a second address and outputting the second address (Figure 3A, Reference 320; C 2, L

35-41); and address output means for inputting the second address and outputting the second

address to an external device (Figure 3a, Reference 220 – the second address is output to any

external device coupled to Reference 122, refer to Figure 1A), wherein the address translation

means stores an external device control information for controlling the external device in

association with at least either one of the first address or the second address and outputs the

external device control information to the external device via the address outputting means (the

address output from the address out means indicates the external a location at which a control

operation will take place such as a read/write operation and thus the address information is

control information). Sharma does not disclose the external control information as information

specifying at least one of an access timing, a memory attribute, and a bus width of the device.

However, Takagi teaches the concept of an address translation means (comprised of References

AT and PMT in Figure 1; C 5, L 42-49; C 6, L 7-9) storing external device control information

in association with a first or second address which specifies at least one of an access timing, a

memory attribute, and a bus width of the device (C 6, L 4-7; C 14, L 33-36; C 12, L 49-68; C 13,

L 1-64). This feature taught by Takagi provides flexibility by allowing data transfers of different

bus widths. Hence, it would have been obvious to one of ordinary skill in the art to use Takagi's

teachings with the system taught by Sharma for the desirable purpose of flexibility.

Regarding claims 5 and 30, Sharma discloses the second address output from the address output

means is input to the address output means via a cache memory and a bus (memory within

Reference 120 which stores the page tables for address translation).

4.   Claims 2-4 and 27-29 are rejected under 35 U.S.C. 103 (a) as being unpatentable over

Sharma et al. (USPN: 5,960,463) and Takagi (USPN: 5,440,708) in view of Richter (USPN:

5,905,885).

Regarding claims 2-3 and 27-28, Sharma and Takagi disclose the limitations stated above in claim 1, however, Sharma and Takagi do not disclose the external device having a PCMCIA interface. Richter teaches the concept of an external device having a PCMCIA interface (Figure 1A; C 1, L 28-37). Richter teaches that PCMCIA is a standard interface and specification to allow PCMCIA cards to vary the capabilities of a computer system thereby intrinsically providing flexibility to the system. Hence, it would have been obvious to one of ordinary skill in the art to use a device having a PCMCIA interface in the system taught by Sharma and Takagi for the desirable purpose of flexibility.

Regarding claims 4 and 29, Sharma and Takagi disclose the limitations cited above, however, Sharma and Takagi do not disclose the CPU, address translation means, address output means and a PCMCIA interface in a second external device formed on the same semiconductor substrate. However, Richter discloses these features (Figure 1, Reference 100 [substrate comprises the elements], Reference 143 comprises the address translation and address output means, Reference 140 and Reference 106). This implementation is provided to achieve certain design goals as is the case with any design implementation. Hence, it would have been obvious to one of ordinary skill in the art to use Richter's teachings with the teachings of Sharma and Takagi for the desirable purpose of achieving the design goals afforded by this specific design organization.

5.   Claims 7-8, 10-11, 34-35 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luick (USPN: 6,349,362) in view of Takagi (USPN: 5,440,708).

Regarding claims 7 and 34, Luick discloses a first address output by a CPU (address output from

Reference 108 in Figure 1); address translation means for translating the first address to a second

address (translation logic within Reference 118 in Figure 1 – the DASD interface inherently

translates the address from the CPU into a cylinder/sector/track format for the DASD device);

and address output means (comprised of References 114, logic within Reference 106 which

initiates a L2 cache access in response to a L1 cache miss and the means coupling References

118 and 104) for outputting an address to both a first external device (Figure 1, Reference 116)

and a second external device (Figure 1, Reference 104), wherein the first address is output to the

first external device via the address output means, the address output means outputs first external

device control information (read/write control lines via Reference 114 and logic within

Reference 106 which initiates a L2 cache access in response to a L1 cache miss) stored in the

address output means in association with the first address, together with the first address to the

first external device (C 5, L 40-42; C 7, L 46-67) and when the second address is output to the

second external device via the address output means, the address output means outputs (via the

means coupling References 118 and 104) second external device control information (read/write

control lines), stored in the address translation means in association with either the first address

or the second address, together with the second address to the second external device (C 4, L 66-

67; C 5, L 1-6). Luick does not disclose the external control information as information

specifying at least one of an access timing, a memory attribute, and a bus width of the device.

However, Takagi teaches the concept of an address translation means (comprised of References

AT and PMT in Figure 1; C 5, L 42-49; C 6, L 7-9) storing external device control information

in association with a first or second address which specifies at least one of an access timing, a

memory attribute, and a bus width of the device (C 6, L 4-7; C 14, L 33-36; C 12, L 49-68; C 13,

L 1-64). This feature taught by Takagi provides flexibility by allowing data transfers of different

bus widths. Hence, it would have been obvious to one of ordinary skill in the art to use Takagi's

teachings with the system taught by Luick for the desirable purpose of flexibility.

Regarding claims 8, 11, 35 and 38, Luick and Takagi disclose the limitations cited above,

however, Luick and Takagi do not disclose the second external device having a PCMCIA

interface. However, it is well known in the art to interface a computer to different interfaces

such as PCI, PCMCIA, ISA to allow the computer to access the devices connected to the

interfaces. Thus it would have been obvious to one of ordinary skill in the art to include an

external device having a PCMCIA interface to the system taught by Luick and Takagi for the

desirable purpose of expandability [by expanding the accessibility of the computer to devices

having a PCMCIA interface].

Regarding claims 10 and 37, Luick and Takagi disclose the second address input to the address

output means via a cache memory and a bus (Luick - memory within Reference 118 which stores

the information, such as table/directory for address translation).

6.   Claims 12 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luick

(USPN: 6,349,362) and Takagi (USPN: 5,440,708) as applied to claims 8 and 35 and further in

view of Richter et al. (USPN: 5,905,885).

Luick and Takagi disclose the limitations cited above, however, Luick and Takagi do not

disclose the CPU, address translation means, address output means and a PCMCIA interface in a

second external device formed on the same semiconductor substrate. However, Richter discloses

these features (Figure 1, Reference 100 [substrate comprises the elements], Reference 143

comprises the address translation and address output means, Reference 140 and Reference 106).

This implementation is provided to achieve certain design goals as is the case with any design

implementation. Hence, it would have been obvious to one of ordinary skill in the art to use

Richter's teachings with the teachings of Luick for the desirable purpose of achieving the design

goals afforded by this specific design organization.

7.   Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the

submitted prior art Kenzo (Japan – 63-296158) in view of Richter (USPN: 5,905;885).

Kenzo discloses a data processor (comprised of conversion means [Abstract] and Reference 1 in

Figure 1) connected via a system bus (Figure 1, Reference 2); a device having an interface

(Figure 1, any one of References M1-M7); wherein the data processor keeps control information

(data width) of the device in an address translation buffer (conversion means) provided in the

data processor, which translates an address necessary to access the device by the address

translation buffer at the time of accessing the device and controls the device in accordance with

the control information kept in the address translation buffer (Abstract). Kenzo does not

explicitly disclose a device having a PCMCIA interface and thus does not disclose storing

control information for a PCMCIA device. However, Richter teaches the concept of a device

having a PCMCIA interface (Figure 1A; C 1, L 28-37). Richter teaches that PCMCIA is a

standard interface and specification to allow PCMCIA cards to vary the capabilities of a

computer system thereby intrinsically providing flexibility to the system. Hence, it would have

been obvious to one of ordinary skill in the art to use a device having a PCMCIA interface in

Kenzo's system and thereby store PCMCIA control information in the address translation buffer,

for the desirable purpose of flexibility.

8.   Claims 15, 17 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Luick (USPN: 6,349,362) in view of Richter (USPN: 5,905,885).

Regarding claims 15 and 32, Luick discloses a CPU for outputting a first address (address output

from Reference 108 in Figure 1); address translation means for inputting the first address,

translating the first address to a second address and outputting the second address (translation

logic within Reference 118 in Figure 1 – the DASD interface inherently translates the address

from the CPU into a cylinder/sector/track format for the DASD device); and address output

means (comprised of References 114, logic within Reference 106 which initiates a L2 cache

access in response to a L1 cache miss and the means coupling References 118 and 104) for

inputting the second address and outputting the second address to an external device (Figure 1,

Reference 104); wherein the address translation means stores an external device control

information (read/write control information) for controlling the external device in association

with at least either one of the first address or the second address, wherein the first address is

input to the address translation means (via Reference 119), the address translation means outputs

the external device control information to the address output means based on the first address or

the second address translated based on the first address (C 4, L 66-67; C 5, L 1-6) and address

output means for outputting the external device control information to the external device (via

the means coupling References 118 and 104). Luick does not disclose the external device having

a PCMCIA interface. Richter teaches the concept of an external device having a PCMCIA

interface (Figure 1A; C 1, L 28-37). Richter teaches that PCMCIA is a standard interface and

specification to allow PCMCIA cards to vary the capabilities of a computer system thereby

intrinsically providing flexibility to the system. Hence, it would have been obvious to one of

ordinary skill in the art to use a device having a PCMCIA interface in Kenzo's system and

thereby store PCMCIA control information in the address translation buffer, for the desirable

purpose of flexibility.

Regarding claim 17, Luick and Richter disclose the CPU and the PCMCIA interface in the

external device formed on the same semiconductor substrate (Richter - Figure 1, Reference 100

[substrate comprises the elements]).

9.   Claims 16 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luick

(USPN: 6,349,362) in view of Richter (USPN: 5,905,885) as applied to claims 15 and 32 above

and further in view of Takagi (USPN: 5,440,708).

Luick and Richter do not disclose the external control information as information specifying at

least one of an access timing, a memory attribute, and a bus width of the device. However,

Takagi teaches the concept of an address translation means (comprised of References AT and

PMT in Figure 1; C 5, L 42-49; C 6, L 7-9) storing external device control information in

association with a first or second address which specifies at least one of an access timing, a

memory attribute, and a bus width of the device (C 6, L 4-7; C 14, L 33-36; C 12, L 49-68; C 13,

L 1-64). This feature taught by Takagi provides flexibility by allowing data transfers of different

bus widths. Hence, it would have been obvious to one of ordinary skill in the art to use Takagi's teachings with the system taught by Luick for the desirable purpose of flexibility.

10.   Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (USPN: 5,960,463) in view of the submitted prior art Kenzo (Japan – 63-296158). Sharma discloses a CPU for outputting a virtual address (Figure 2A- logic within Reference 120 which provides an address to Reference 210); first address translation means and second address translation means for inputting the virtual address, translating the virtual address to a physical address and outputting the physical address (Figure 2A, References 275 and 235); and external bus control means for inputting the physical address and outputting to an external device (Figure 2A, References 220 and 122); selection logic for selecting information output from the first address translation means or the second address translation means (Figure 2A, Reference 260). Sharma does not disclose the first and second address translation means storing external device control information for controlling the external device in association with either the first address or the second address and selection means for selecting the external device control information output from the first address translation means or the second address translation means. However, Kenzo teaches the concept of storing external device control information (data width) in an address translation means (Abstract). Kenzo discloses that this feature improves processing efficiency (Abstract) particularly in system with peripheral (external devices) having different data widths. Hence, it would have been obvious to one of ordinary skill in the art to use Kenzo's teachings in the system taught by Sharma [with external devices having different data widths] for the desirable purpose of efficiency.

11.   Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al.

(USPN: 5,960,463) in view of the submitted prior art Kenzo (Japan – 63-296158) as applied to

claim 22 above and further in view of Takagi (USPN: 5,440,708).

Sharma and Kenzo do not disclose the external control information as information specifying at

least one of an access timing, a memory attribute, and a bus width of the device. However,

Takagi teaches the concept of an address translation means (comprised of References AT and

PMT in Figure 1; C 5, L 42-49; C 6, L 7-9) storing external device control information in

association with a first or second address which specifies at least one of an access timing, a

memory attribute, and a bus width of the device (C 6, L 4-7; C 14, L 33-36; C 12, L 49-68; C 13,

L 1-64). This feature taught by Takagi provides flexibility by allowing data transfers of different

bus widths. Hence, it would have been obvious to one of ordinary skill in the art to use Takagi's

teachings with the system taught by Sharma and Kenzo for the desirable purpose of flexibility.

Response to Arguments

12.   Applicant's arguments with respect to the claims have been considered but are moot in

view of the new ground(s) of rejection.

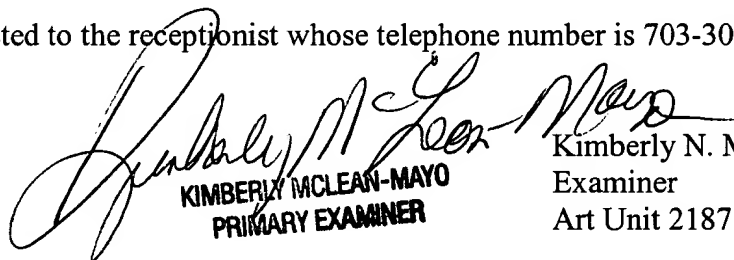## *Allowable Subject Matter*

13.   Claims 18-21 are allowed.

Conclusion

14.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-

9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-746-7329 for regular

communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is 703-308-2100.

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

March 24, 2004